U.S. DEPARTMENT OF ENERGY

Basic Research Needs for Microelectronics Workshop

Briefing to ASCAC

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September 18, 2018

Basic Research Needs for Microelectronics Workshop

Co-sponsored by ASCR, BES, HEP; October 23 – 25, 2018

Workshop Chair: Cherry Murray (Harvard Univ.)
Associate Chairs: Supratik Guha (ANL)
Dan Reed (Univ. of Utah)

Technology Liaison: Gil Herrera (SNL)
SC Technical Leads: Andy Schwartz (BES)
Robinson Pino (ASCR)
Eric Colby (HEP)



CHARGE:

- Conduct a thorough assessment of critical scientific challenges, fundamental research opportunities, and priority research directions that require further study as a foundation for future advances in microelectronics over the next decade and beyond.
- Emphasize energy-relevant applications and those areas that are aligned with the missions and needs of the DOE Offices of Advanced Scientific Computing Research (ASCR), Basic Energy Sciences (BES), and High Energy Physics (HEP) including data management and processing, power electronics, and high performance computing.
- Examine research that is relevant to both the extension of CMOS and beyond CMOS technologies; however topics of direct relevance to Quantum Information Science and Quantum Computing are outside the scope of this workshop.
- Focus on a co-design innovation ecosystem in which materials, chemistries, devices, systems, architectures, and algorithms are researched and developed in a closely integrated fashion.

Outline

- Motivation for BRN workshop
- One-day Roundtable held in May 2018
  - Goals, Format, Output
- Planning for October BRN workshop

BRN for Microelectronics Workshop – Motivation

- Semiconductor-based microelectronics are critical to the U.S. economy, scientific advancement, and national security
  - Semiconductor products are currently the third largest class of U.S. exports (behind aircraft and automobiles)
  - U.S. companies account for more than 50% of the world market by revenue
  - Semiconductor industry directly employs ~250,000 people; ~1 million associated jobs
- The decades long success of Moore's Law was driven by innovation
  - Materials and chemical sciences
  - Computer science
  - Electrical engineering
  - Fabrication technologies
- Additional innovation needed to keep up with dramatic market growth

Sources: SIA "Made in America: The Facts about Semiconductor Manufacturing," Aug. 2015
SIA "2014 Factbook", 2014

Innovation Opportunity Space

- Materials Research
- Device Physics
- Design and Fabrication
- Computer Science & Applied Math

- Other Considerations
  - *Outside the box*: Alternative materials, devices, fabrication techniques and architectures are likely to result
  - *Use-inspired science*: Function and application need to be considered at early stages

Future Computing Technologies are Important to DOE
as well as many other Federal Agencies

- High-performance computing & simulation underpin DOE missions in energy, environment, and national security
  - Historical role of computing in DOE
  - DOE/vendor synergies in deploying computing technologies

- Future computing technologies (e.g., quantum, neuromorphic, probabilistic, etc.) hold promise for next-generation DOE mission applications
  - DOE research and facilities (e.g. HEP experiments, ASCR HPC, BES light sources) will depend on advanced computing and sensing technologies
  - Likely will augment, not replace, conventional supercomputing
  - Could open new avenues for use of computing in science (data analytics, machine learning, artificial intelligence, …)

- New directions for applied mathematics and computer science are likely to emerge that could enable new science across DOE-SC

Call To Action

- Significant challenges as CMOS extends below 5nm
- The end to Moore's Law will impact U.S. industry and competitiveness
- The importance of this issue and its technical complication will require *innovative approaches* to keep the U.S. in a leadership position
- Solving a problem of this scale will require *"whole of government"* approach and a robust *public/private partnership* to apply the best research from *industry, academia and government research facilities* to allow the U.S. to successfully make this technology transition
- DOE, and particularly the Office of Science, will play a significant role in this effort
- DOE-SC was charged with organizing a *Basic Research Needs Workshop* to define the highest priority research directions

Microelectronics BRN Scoping Roundtable – Goal

May 18, 2018

- Convene a small group of experts from industry, academia, and national labs to **discuss most critical scientific knowledge gaps that will impede progress in microelectronics technology of the next decade.**
- Identify a group of 3-5 topical areas in which fundamental research over the next 5-10 years could result in significant impact on microelectronics technology, with an emphasis on areas aligned with DOE-SC capabilities and needs.
- **Use the output of the Roundtable to define the scope for a BRN workshop to be held in Fall 2018.**

Microelectronics BRN Scoping Roundtable – Format

May 18, 2018

- Chaired by Gil Herrera of SNL
- 17 Participants from Academia, Industry, Labs
- Introductory remarks by DOE-SC leadership
- Each participant asked to present the following:
  - A brief statement of your background as it relates to the development of advanced microelectronics
  - From your personal perspective or that of your organization, an overview of the most critical roadblocks, knowledge gaps, research needs, and opportunities related to the development of microelectronics over the next decade.
- Discussion of common themes

Microelectronics BRN Scoping Roundtable – Output

May 18, 2018

- Notes from the meeting summarized the common themes, including the following:
  - Materials
  - Device physics
  - Emerging architectural approaches and 3D integration
  - Crosscutting: Metrology, energy efficiency, and manufacturability
- A list of potential questions to be addressed at the BRN workshop:
  - What are the materials challenges at the extremes that will enable continued CMOS device performance improvements absent dimensional scaling?
  - What new materials/devices should be explored to enable post-CMOS systems?
  - What new theory must be developed to support device design, modeling, and simulation for post-CMOS devices?
  - What new experimental and measurement techniques will be required to enable thorough materials and device characterization?
  - What new architectures and architectural approaches for High Performance Computing (HPC) will be required to continue performance improvements with CMOS-based computers at the end of scaling? To exploit the advantages of new devices and materials for post-CMOS HPC?
  - What technological opportunities, particularly in areas relevant to Office of Science facilities, are enabled by new devices and materials?

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- Based on output from Roundtable, DOE-SC wrote the Charge for the October BRN workshop and recruited the three chairs
- DOE-SC and the Workshop Chairs developed the scope and structure for the workshop:
  - Breakout Panel 1: *Big Data Collection, Analytics, and Processing for future SC Facilities*
    - Leads: Kerstin Kleese van Dam (BNL), Sayeef Salahuddin (UC Berkeley)
  - Breakout Panel 2: *Co-Design for High Performance Computing beyond Exascale*
    - Leads: Jim Ang (PNNL), Tom Conte (GA Tech)
  - Breakout Panel 3: *Power Control, Conversion, and Detection*
    - Leads: Bob Kaplar (SNL), Debdeep Jena (Cornell)
  - Breakout Panel 4: *Crosscutting Research*
    - Leads: Rick Stevens (ANL), Harry Atwater (Caltech)

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STATUS:

- Chairs identified
- Dates/location finalized
- DOE-SC and Chairs have defined scope/structure for workshop
- Plenary Speakers being recruited
- Panel Leads Confirmed and Participants have been invited
- Report expected in early 2019