Advanced Detectors for Synchrotron Radiation

FWP # LS-015

PI's D. Peter Siddons, Paul O'Connor

Brookhaven National Laboratory
Upton
New York 11973
Outline

- Main thrust: to try to use advanced technologies such as 3D integration for X-ray detector applications
- Two straw-man detector projects
  - XCS (x-ray 'speckle') experiments
  - Imaging + spectroscopy in one detector; HIXD.
- Attempt to develop planar monolithic technology for germanium sensors.
Process flow for 3D CMOS Chip
(Courtesy Ray Yarema, Fermilab)

- 3 tier chip (tier 1 may be CMOS)
  - 0.18 um (all layers)
  - SOI simplifies via formation
- Single vendor processing

1) Fabricate individual tiers

2) Invert, align, and bond wafer 2 to wafer 1

3) Remove handle silicon from wafer 2, etch 3D Vias, deposit and CMP tungsten

4) Invert, align and bond wafer 3 to wafer 2/1 assembly, remove wafer 3 handle wafer, form 3D vias from tier 2 to tier 3
X-ray Photon Correlation Spectroscopy (XPCS):

Replace with VIPIC ROIC and sensor.

VIPIC

Fermilab ASIC Group, USA
Grzegorz Deptuch, Marcel Trimpl, Raymond Yarema

AGH UST, POLAND
Pawel Grybos, Robert Szczygiel,
PhD students: Maciej Kachel, Piotr Kmon
VIPIC (Vertically Integrated Photon Imaging Chip)

- **Specifications**
  - 64 x 64 array of 80 micron pixels
  - Dead timeless operation
  - Sparsified data readout
  - Binary readout (no energy information)
  - High speed frame readout time (10 usec min for occupancy ~ 100 photons/cm²/usec)
  - Optimized for photon energy of 8KeV
  - Triggerless operation

- **Features (5.5 x 6.3 mm die size)**
  - Two 5 bits counters/pixel for dead timeless recording of multiple hits per time slice (imaging mode)
  - Address generated by circuit without hard coding
  - Constant pixel address readout time (5 ns) regardless of hit pixel location by means of binary tree principle.
  - Parallel serial output lines
    - 16 serial high speed LVDS output lines
    - Each serial line takes care of 256 pixels
  - 2 tier readout chip with separate analog and digital sections
  - Adaptable to 4 side buttable X-ray detector arrays
VIPIC Block Diagram

- 16 Serial Output Lines (LVDS)
- Preamp X6
- Discriminator (Disc.)
- ts=250 ns
- Program latches
- Two 5 bit counters
- Serializer and LVDS Output
- Sparsification
- Serial Output Line
Pixel Tier Layouts and Sensor Mounting Options

Option 1 - Less Aggressive Mounting
- ROI C to Sensor uses Direct bond interconnect
- Sensor with wire bond fanout (300 um)
- Sensor to PCB uses bump bonds

Option 2 - More Aggressive Mounting
- ROI C is 25 um thick after thinning
- for four side butttable sensor arrays
Status

- CMOS wafers fabricated (1.5 years from submission!)
- CMOS 2-layer bonding done
- Sensors fabricated
- Waiting for CMOS finishing and singulation
Real-time autocorrelator

- VIPIC generates a sparsified stream of photon events. The scientific content of this stream is in its temporal correlations. Since each pixel needs its own correlator, we need to build 4096 autocorrelators to process one VIPIC detector block.

- We have implemented two blocks of 256 multiple-Tau autocorrelators in a single FPGA. Implementation as a CMOS ASIC would allow us to fit 4 such blocks in a chip. Thus only 4 chips would treat one VIPIC block.
Implementation

- The table shows the resources consumed by the 256-correlator block. It is limited by the simple gate count. An ASIC would accommodate these much more efficiently.

<table>
<thead>
<tr>
<th>Logic Utilization</th>
<th>Used</th>
<th>Available</th>
<th>Utilization</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Slice Registers</td>
<td>98141</td>
<td>301440</td>
<td>32%</td>
</tr>
<tr>
<td>Number of Slice LUTs</td>
<td>146540</td>
<td>150720</td>
<td>97%</td>
</tr>
<tr>
<td>Number of fully used LUT-FF pairs</td>
<td>46818</td>
<td>197863</td>
<td>23%</td>
</tr>
<tr>
<td>Number of bonded IOBs</td>
<td>0</td>
<td>600</td>
<td>0%</td>
</tr>
<tr>
<td>Number of BUFG/BUFGCTRLs</td>
<td>13</td>
<td>32</td>
<td>40%</td>
</tr>
<tr>
<td>Number of DSP48E1s</td>
<td>24</td>
<td>768</td>
<td>3%</td>
</tr>
</tbody>
</table>
HIXD: A Hyperspectral Imaging X-ray Detector

• We are often asked if it is possible to make an imaging detector with per-pixel spectroscopic capability.

• We have begun designing such a detector. We will begin with the low-noise analog section and eventually add a second digital layer to process the digitized photon pulse heights.

• Our initial study indicates that a high-performance spectrometer should be possible in a pixel size of order 100-200 um.
Low-noise pixel electronics

- The pixel architecture contains a low-noise current preamplifier, a multiplexor and ADC, and logic to trigger conversion of neighboring pixels in the case that a charge-shared event is detected.

- The front-end design is based on low-noise amplifiers successfully used by the BNL microelectronics group for several earlier designs.
The above curves summarize the simulated performance of the low-noise preamp and shaper. The left-hand set of curves show the shaped output at several shaping times, while the right-hand figure shows that an ENC of around 10 electrons RMS is achievable at a modest shaping time.
Transistor-level layout

- Lithography mask designs for the preamp / shaper in two technologies, TSMC and IBM. Both are based on 130 nm design rules. The IBM version is slightly more compact.

- The lower figure is a low-power 10-bit current-mode ADC suitable for use in the design, servicing several pixels via a multiplexor.
Studying charge-sharing

- Small pixel $\rightarrow$ Charge sharing
- Shared charges must be recombined
- These test diode arrays can be connected to Maia electronics
- Hexagonal (3 neighbors) and square (4 neighbors)
- Issues and algorithms for recombination can be investigated before pixelated ASIC is ready.
Planar process for Germanium

• We would like to have a process capable of making sensors based on germanium.

• Issues
  
  • Ge oxide is unstable and water-soluble
    – No use as a barrier or passivation layer; key for silicon structures
  
  • Can't use standard Si processing steps
    – Any oxidizing aqueous solution will eat germanium
    – Thermal budget is much more restricted than for Si.
  
  • Different contact technology
Passivation layer

- Industry has been using “Hi-K dielectrics with germanium-rich devices
- We have studied HfO2 as a potential passivation layer for pure germanium
- We have shown that it forms high-resistance, low-defect layers on germanium
- We have measured its band alignment with that of germanium. It is well-positioned to block electron and hole transport.
Device fabrication

- “N in P” diodes (we have P-type wafers)
- Hi-K passivation layer
- P-spray to define surface potentials
- N implants to form junctions.
- 3” wafer mask set containing test structures, 1mm^2 diodes and 0.125mm x 4mm microstrip arrays.
Collaborators

G. De Geronimo, Neena Nambiar, Shaorui Li, P. Rehak, R. Beuttenmuller, G. Carini, A. Rumaiz, E. Huey, J. Woicik, Zhi Yong Li,
Brookhaven National Laboratory, Upton, NY 11973, USA

G. Deptuch, Marcel Trimpl, R. Yarema, R. Lipton
Fermilab, Batavia, IL 60510

P. Grybos, R. Szczygiel, M. Kachel, P. Kmon
AGH-UST, Krakow, Poland.